Amendments to the Specification

Please replace paragraph [00037] beginning on page 10, line 3 with the following rewritten paragraph:

Digital pot 208 receives various inputs from system 200B, including, input 301, which is used to control the up/down ("U/D") pin (320) (i.e. toggle pin 3 of digital pot 208). Another input 302 is used to control the chip select (also referred to as "CS") (pin 4 (322) of digital pot 208). Input 302 addresses digital pot 208 and enables resistance change, as described below.

Please replace paragraph [0038] beginning on page 10, line 10 with the following rewritten paragraph:

Digital pot 208 receives input voltage at pin 1 (318) (Vdd 304) and is grounded at pin 2 (303). To illustrate one aspect of the present invention, Vdd may be 3.3V. It is noteworthy that the adaptive aspects of the present invention are not limited to any particular voltage at pin 6 (326) or pin 1 (318).

Please replace paragraph [00039] beginning on page 10, line 16 with the following rewritten paragraph:

Resistor R1 305 acts as a "pull down" resistor forming a voltage divider with digital pot 208 pin L (324) (i.e. pin 5). To illustrate one aspect of the present invention, R1 305 may be 4.7K. It is noteworthy that the adaptive aspects of the present invention are not limited to any particular resistance value of R1 305.

Please replace paragraph [0040] beginning on page 10, line 22 with the following rewritten paragraph:

NVRAM 205 receives signals 308-310 from system 200B. Signal 308 is a clock signal received at pin 2 (330), signal 309 is a chip select signal received at pin 1 (332) and signal 310 is a "data-in" signal received at pin 3 (334) that allows data content to be written in NVRAM 205. The foregoing signals allow system 200B to access NVRAM 205.

Please replace paragraph [00041] beginning on page 11, line 3 with the following rewritten paragraph:

NVRAM receives signal 306 (EE_PE) at pin 6 (336) that enables system 200B firmware to write to NVRAM 205.

Please replace paragraph [00042] beginning on page 11, line 5 with the following rewritten paragraph:

At power on of system 200B, digital pot 208 is set somewhere in the mid-point of its resistance range. In the foregoing illustration, that will be around 25K-ohm value, which will be the resistance between pin 6 (326) and 5 (324) of digital pot 208. At power up, R1 305 forms a voltage divider, and voltage at pin 5 (324) of digital pot 208 is given by:

Please replace paragraph [00043] beginning on page 11, line 12 with the following rewritten paragraph:

Vdd * (R1/(R1 + R2)), where R1 is resistor 305 and R2 is the resistance of the digital pot 208 at power up (in the foregoing example, 25 K-ohm). If Vdd is 3.3V and R1 305 is 4.7K-ohm, the voltage at pin 5 (324) of digital pot 208 is 0.16Vdd, i.e. 0.52V. This voltage

or voltage similar to this is applied to pin 6 (323) of NVRAM 205. This disables the ability to write to NVRAM 205.

Please replace paragraph [00044] beginning on page 11, line 20 with the following rewritten paragraph:

To enable writes, firmware running on system 200B drives GPIO pins (signals 301 and 302) to decrease the resistance between pins 5 (324) and 6 (326) of digital pot 208. Firmware commands digital pot 208 to change resistance a certain way (i.e. up or down) by driving signals 301 and 302. When signal 302 goes from high to low and signal 301 is low, decrement mode is selected enabling the resistance to decrease. When signal 302 goes from high to low and signal 301 is high, increment mode is selected enabling resistance to increase.

Please replace paragraph [00046] beginning on page 12, line 8 with the following rewritten paragraph:

Thereafter, pin 3 (320) is toggled, which steps wiper 312, changing the resistance between pins 5 (324) and 6 (326). The goal is to reach a certain voltage divider output, Y volts (for example, 0.7Vdd) to enable writes to NVRAM 205 after power up and/or reset.

Please replace paragraph [00048] beginning on page 11, line 18 with the following rewritten paragraph:

The chances of random toggling of ASIC 200B control pins to enable the decrement mode (or increment mode if digital pot 208 is configured as a potentiometer) of digital pot 208, then toggle the UP/DN pin (320) 15 times while remaining in decrement mode, is very

small, and this minimizes the chances of NVRAM from getting corrupted at power up and/or reset.

Please replace paragraph [00052] beginning on page 13, line 15 with the following rewritten paragraph:

In step S403, system 200B commands digital pot 208 to change the resistance between pins 5 (324) and 6 (326) by driving signals 301 and 302. To decrease the resistance, signal 301 is low and signal 302 is brought from high to low. Signal 301 is then toggled so that wiper 312 changes the resistance between pins 5 (324) and 6 (326).

Please replace paragraph [00053] beginning on page 13, line 22 with the following rewritten paragraph:

In step S404, once the resistance between pins 5 (324) and 6 (326) is low, signal EE-PE 306 is enabled, which allows firmware of ASIC 200B to write to NVRAM 205, using signals 308-310.